substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate oxide layer on the trench sidewalls and the bottom wall of the first trench;

a gate conductor disposed within the first trench to a depth of at least an elevation of the upper surface of the substrate;

a vertically-oriented layer of semiconductor material extending upwardly along the gate oxide layer on the side thereof opposite the first trench, the vertically-oriented layer extending from the body layer to the upper surface of the substrate, the vertically-oriented layer comprising a first vertical layer portion contiguous with the body layer doped with said first polarity dopant to define an active body region including a vertical channel, and a second vertical layer portion atop the first vertical layer portion and forming a PN junction therewith, the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region; and

a vertically-extending source conductor contacting the vertically-oriented layer on a side thereof opposite the gate oxide layer and gate conductor, the source conductor electrically shorting the source region to the active body region across the PN junction;

the gate conductor comprising doped polysilicon contacting the gate oxide layer within the trench and [a gate metal layer coextending over the doped polysilicon].

44. (New) A recessed gate field effect power MOS device according to claim 43 further comprising:

an insulating layer over the gate conductor; and

an upper metal layer over the insulating layer and [contacting the gate conductor through a via in the insulating layer].

45. (New) A recessed gate field effect power MOS device according to claim 44 wherein [a portion of the upper metal layer over [the insulative layer] contacts the source

conductor in electrical isolation from the gate conductor.

46. (New) A recessed gate field effect power MOS device according to claim 43 further comprising:

an insulating layer over the gate conductor; and

an upper metal layer over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer.

47. (New) A recessed gate field effect power MOS device according to claim 43 in which the first vertical layer portion has a lateral thickness less than a vertical height thereof.

48. (New) A recessed gate field effect power MOS device according to claim 43 in which the first vertical layer portion has a lateral thickness less than 1 μm.

49. (New) A recessed gate field effect power MOS device according to claim 48 in which the first vertical layer portion contiguous with the body layer is doped to a first doping concentration and a laterally-extending portion of the body layer subjacent the first vertical layer portion has at least a top portion doped to a second doping concentration greater than the first doping concentration.

50. (New) A recessed gate field effect power MOS device according to claim 43 including a vertically-oriented sidewall spacer extending upward from the upper surface of the substrate atop the vertically-oriented layer .

51. (New) A recessed gate field effect power MOS device according to claim 50 including one of said vertically-oriented layer on each side of the trench, each having one of said vertically-oriented sidewall spacer thereon, and an insulative layer extending laterally between the sidewall spacers over the gate conductor.

52. (New) A recessed gate field effect power MOS device according to claim 51 including an upper metal layer extending over the insulative layer and the sidewall spacers and contacting the vertically-extending source conductor.

53. (New) A recessed gate field effect power MOS device according to claim 43 in which the vertically-extending source conductor contacts a laterally-extending portion of the body layer at a position spaced below the PN junction.

54. (New) A recessed gate field effect power MOS device according to claim 53 in which the first vertical layer portion is doped to a first doping concentration defining a threshold voltage of the channel and the laterally-extending body layer is doped to a second doping concentration greater than the first doping concentration.

55. (New) A recessed gate field effect power MOS device according to claim 43 in which the first trench and the gate oxide layer and gate conductor within the trench form a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands, each of said plurality containing a downward extending finger of source conductor surrounded by a portion of the active body region including said vertical channel, the channel having a width defined in each island by a perimetral length of the island.

56. (New) A recessed gate field effect power MOS device according to claim 43 wherein the first trench, the gate oxide layer and the gate conductor together form a gate structure configured as a finger, said recessed gate field effect power MOS device comprising a plurality of said finger;

the source conductor intermediate the fingers of said plurality to define an interdigited source-gate structure.

57. (New) A recessed gate field effect power MOS device according to claim 43 including at least two of said first trench spaced laterally apart with two of said vertically-oriented layer of semiconductor substrate defining a second trench between the two of said first trench, each first trench containing the gate oxide layer and gate conductor, said source conductor extending into the second trench and contacting the bottom of the second trench and the respective sides of the two vertically-oriented layers.

58. (New) A recessed gate field effect power MOS device according to claim 43 in which the substrate includes a base layer of said first polarity dopant such that the device defines an alternating PNPN four-layer structure wherein the body layer defines a base of an upper bipolar transistor and a collector of a lower bipolar transistor.

59. (New) A recessed gate field effect power MOS device according to claim 43 in which the gate oxide layer includes a first portion having a first thickness in a lower portion of the trench and a second portion having a second thickness in an upper portion of the trench, the first thickness being greater than the second thickness.

60. (New) A recessed gate field effect power MOS device according to claim 43 wherein the gate metal layer comprises aluminum.

61. (New) A recessed gate field effect power MOS device according to claim 43 wherein the gate metal layer comprises a plateable metal.

62. (New) A recessed gate field effect power MOS device according to claim 43 wherein the gate conductor comprises a refractory metal silicide over the doped polysilicon, and beneath the gate metal layer.

63. (New) A recessed gate field effect power MOS device according to claim 62 wherein the gate metal layer comprises a plateable metal.

64. (New) A recessed gate field effect power MOS device according to claim 62 wherein the gate metal layer comprises aluminum.

65. (New) A recessed gate field effect power MOS device according to claim 60 wherein the upper metal layer comprises aluminum.

66. (New) A recessed gate field effect power MOS device according to claim 60 wherein the insulating layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass, and phosphosilicate glass (PSG).

67. (New) A vertical double-diffused insulated gate transistor, comprising:

a substrate comprising silicon with doping of a first dopant type;

a gate oxide layer disposed over the surface of the substrate;

a gate conductive layer on the gate oxide layer, the gate oxide layer and the gate conductive layer collectively defining an opening of a defined outline characteristic;

double-diffused dopant means of opposite second and first dopant types disposed within the substrate to define first and second PN junctions spaced laterally apart under the oxide layer and contoured in accordance with the defined outline characteristic, the PN junctions arranged to define portions of a field effect transistor, the portions including a source region of the first dopant type in the substrate subjacent the defined outline characteristic and bounded by the first PN junction, a drain region of the first dopant type bounded by the second PN junction and spaced laterally from the defined outline characteristic and extending downwardly into the substrate, and a body region of the second dopant type extending between the first and second PN junctions with a channel portion thereof underlying the oxide layer and the gate conductive layer, the channel portion operable under field effect to conduct current between the source and drain regions; and

a source conductive layer on the upper surface of the substrate and contacting the source region within said opening, the source conductive layer spaced apart and electrically separate from the gate conductive layer;

the gate conductive layer comprising doped polysilicon on the gate oxide layer and a metal layer coextending over the doped polysilicon.

68. (New) A device according to claim 67, wherein the region of the second dopant type of the dopant means comprises a first portion and a second portion, the first portion disposed alongside the source region and having a first doping concentration, the second portion contained within the first portion and extending laterally beneath the source

conductive material, the second portion having a second doping concentration greater than the first doping concentration.

69. (New) A device according to claim 67, further comprising insulative sidewall spacers extending outwardly from the substrate surface along the defined outline characteristic, the sidewall spacers laterally separating the gate conductive layer and the source conductive layer.

70. (New) A device according to claim 67, further comprising a low-resistivity contact layer between the source region and the source conductive layer.

71. (New) A device according to claim 69 wherein the metal layer of the gate conductive layer is aligned with the doped polysilicon between the sidewall spacers.

72. (New) A device according to claim 67 wherein the source conductive layer comprises aluminum.

73. (New) A device according to claim 67, wherein the metal layer of the gate conductive layer comprises aluminum.

74. (New) A device according to claim 73, wherein the source conductive layer comprises aluminum.

75. (New) A device according to claim 73, further comprising:

a dielectric layer disposed over the gate conductive layer; and

metallization disposed over the dielectric layer and contacting the gate conductive layer through the dielectric layer.

76. (New) A device according to claim 75, wherein the dielectric layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass and phosphosilicate glass (PSG).

77. (New) A device according to claim 75, wherein the dielectric layer comprises first and second layers of dielectric material, the dielectric material of the second layer different from the dielectric material of the first layer.

78. (New) A device according to claim 73 further comprising:

a dielectric layer disposed over the gate conductive layer; and

metallization disposed over the dielectric layer and the gate conductive layer, the metallization contacting the source conductive layer through said dielectric layer.

79. (New) A device according to claim 78, wherein the dielectric layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass and phosphosilicate glass (PSG).

80. (New) A device according to claim 78, wherein the dielectric layer comprises first and second layers of dielectric material, the dielectric material of the second layer different from the dielectric material of the first layer.

81. (New) A device according to claim 67, wherein the metal layer of the gate conductive layer comprises a plateable metal.

82. (New) A device according to claim 81, wherein the plateable metal comprises aluminum.

83. (New) A device according to claim 67, wherein the metal layer of the gate conductive layer comprises refractory metal coextending over the doped polysilicon and plateable metal coextending over the refractory metal.

84. (New) A device according to claim 67, wherein the metal layer of the gate conductive layer comprises refractory metal coextending over the doped polysilicon and aluminum coextending over the refractory metal.

85. (New) A device according to claim 67, wherein the gate conductive layer comprises refractory metal silicide over the doped polysilicon and the metal layer comprises a plateable metal.

86. (New) A device according to claim 85, wherein said plateable metal comprises aluminum.

87. (New) A device according to claim 67, wherein the metal layer of the gate conductive layer comprises first and second layers of metal.

88. (New) A device according to claim 67, wherein a portion of the substrate surface defines a trench, the source region of the ~~double-diffused~~ dopant means meeting a region of the substrate surface associated with the defining trench.

89. (New) A device according to claim 88, further comprising insulative sidewall spacers extending outwardly from the substrate and along the defined outline characteristic, the source conductive layer being confined between walls of the trench and the sidewall spacers and the gate conductive layer outside said sidewall spacers.

90. (New) A device according to claim 89, further comprising a low-resistivity contact layer disposed between the source region and the source conductive layer.

91. (New) A device according to claim 90, wherein the low-resistivity contact layer comprises a shallow diffusion of the same dopant type as the source region.

92. (New) A device according to claim 91, in which the low-resistivity contact layer comprises at least one of a layer of refractory metal and a refractory metal silicide.

93. (New) A device according to claim 67, further comprising:

an insulating layer disposed over the conductive gate layer; and

metal disposed over the insulating layer and contacting the gate conductive layer through the insulating layer.

94. (New) A device according to claim 92, wherein the insulating layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass and phosphosilicate glass (PSG).

95. (New) A device according to claim 94, wherein the insulating layer comprises first and second layers of dielectric material, the dielectric material of the second layer different from the dielectric material of the first layer.

96. (New) A device according to claim 67, further comprising:

an insulating layer disposed over the conductive gate layer; and

metal disposed over the insulating layer and contacting the source conductive layer through the insulating layer.

97. (New) A device according to claim 96, wherein the insulating material comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass and phosphosilicate glass (PSG).

98. (New) A power MOSFET comprising:

a semiconductor substrate, the substrate comprising drain semiconductor material of a first type dopant;

source semiconductor material of a dopant type the same as said first dopant type;

channel semiconductor material of a second dopant type disposed between the source semiconductor material and the drain semiconductor material, the channel semiconductor material operative under field effect to conduct current between the source semiconductor material and the drain semiconductor material;

a conductive gate structure configured to enable provision of a field to the channel semiconductor material;

a gate oxide layer disposed between the conductive gate structure and the channel semiconductor material;

said conductive gate structure comprising doped polysilicon contacting the oxide layer and metal disposed coextensively over the doped polysilicon;

an insulating layer disposed over said gate structure; and

metallization over said insulating layer, the metallization contacting the gate structure through said insulating layer.

99. (New) A power MOSFET according to claim 98 wherein the metal of the conductive gate structure comprises a metal on a refractory metal-silicide.

100. (New) A power MOSFET according to claim 98 wherein the metal of the conductive gate structure comprises plateable metal.

101. (New) A power MOSFET according to claim 100 wherein the insulative layer is deposited at temperature less than 430 C°.

102. (New) A power MOSFET according to claim 98 wherein the gate metal comprises aluminum.

103. (New) A power MOSFET according to claim 98 wherein the metallization over said insulating layer comprises aluminum.

104. (New) A power MOSFET according to claim 98 wherein the source semiconductor material, channel semiconductor material, and drain semiconductor material are configured to define a laterally-oriented channel structure, said lateral orientation parallel to an upper surface of said substrate.

105. A power MOSFET according to claim 104, wherein said conductive gate structure defines a finger; said power MOSFET comprising a plurality of said fingers disposed over said substrate, said plurality laterally separated to define a striped pattern over said substrate.

106. A power MOSFET according to claim 98 wherein the source semiconductor material, channel semiconductor material, and drain semiconductor material are configured to define a vertically-oriented channel structure, said vertical orientation normal to an upper surface of said substrate.

107. A power MOSFET according to claim 106, wherein the conductive gate structure comprises a laterally patterned interconnected matrix enclosing a plurality of islands, said plurality of islands comprising respective said vertically-oriented channel structures; said power MOSFET further comprising source conductor extending downwardly into said plurality of islands, the source conductor contacting the source semiconductor material of respective said vertically-oriented channel structures of said plurality of islands.